



1 / 30

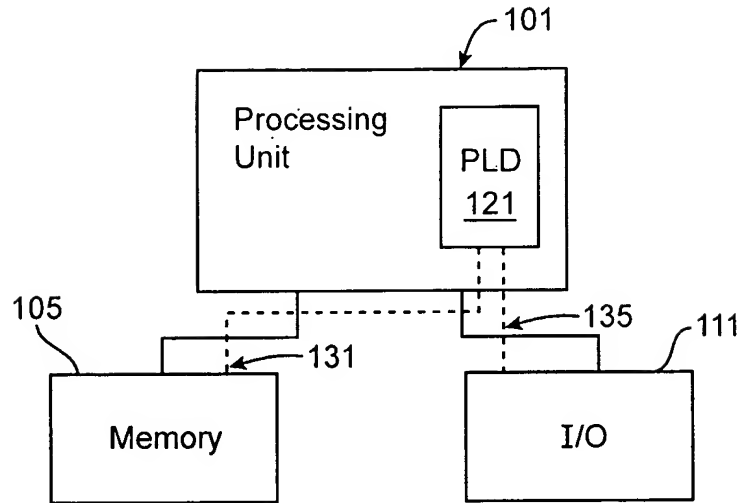


FIG. 1

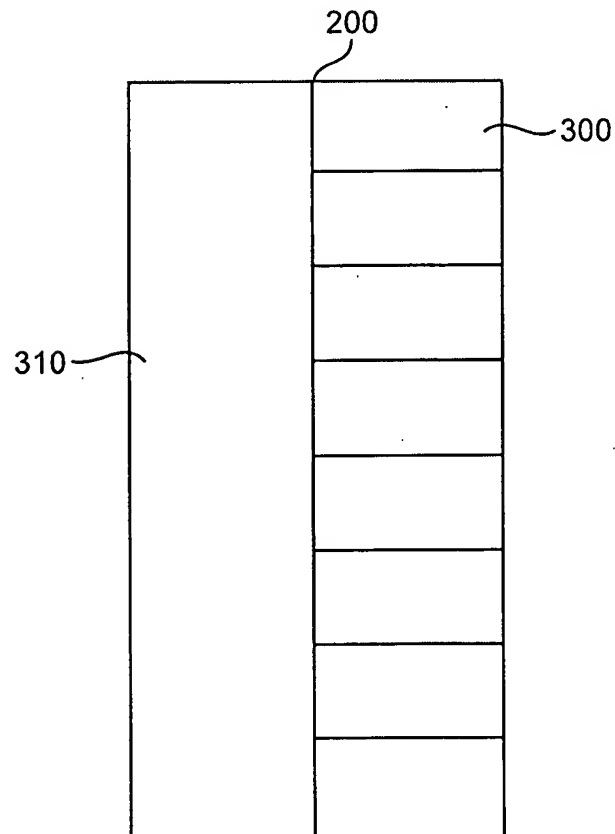


FIG. 3



2 / 30

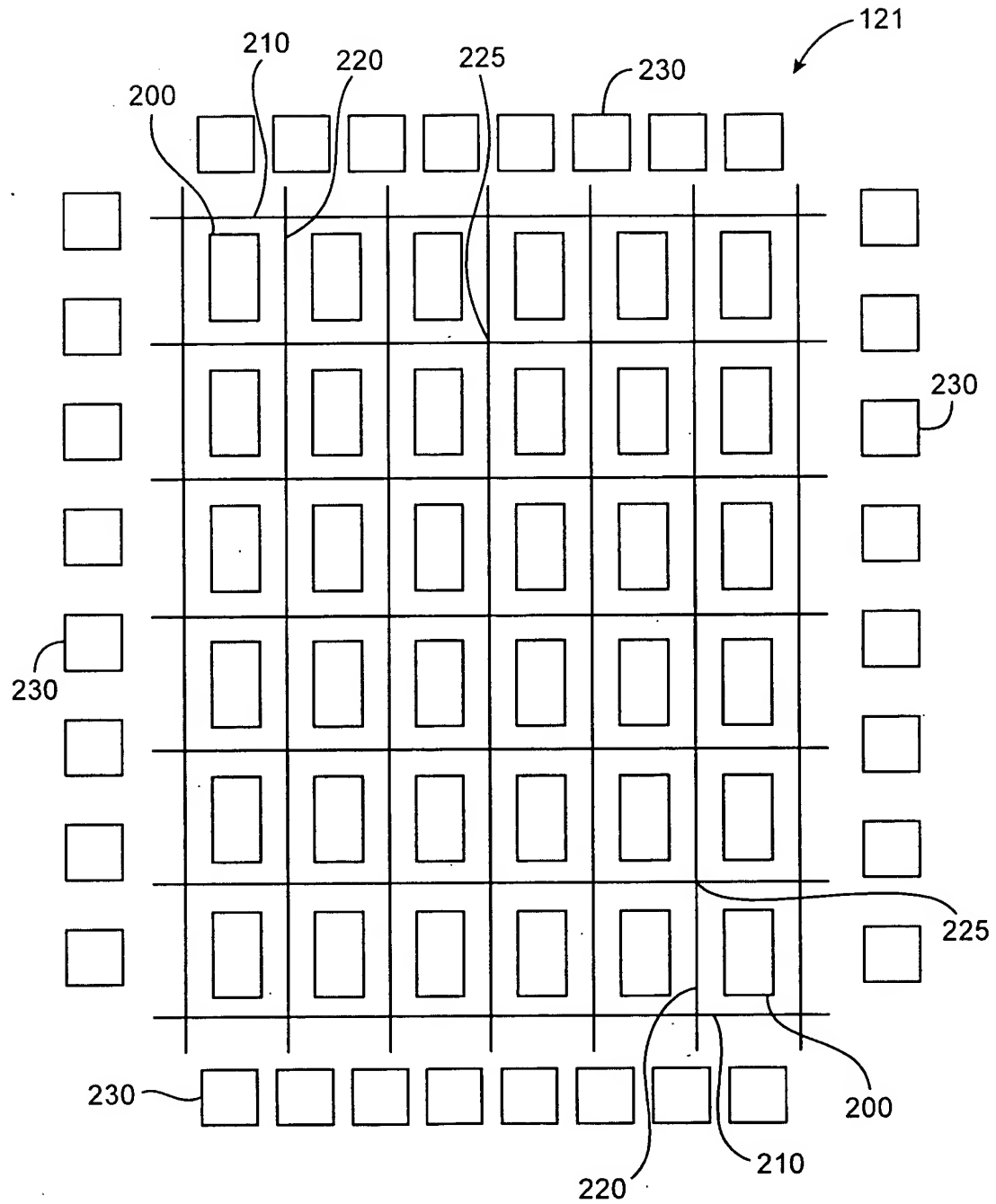


FIG. 2



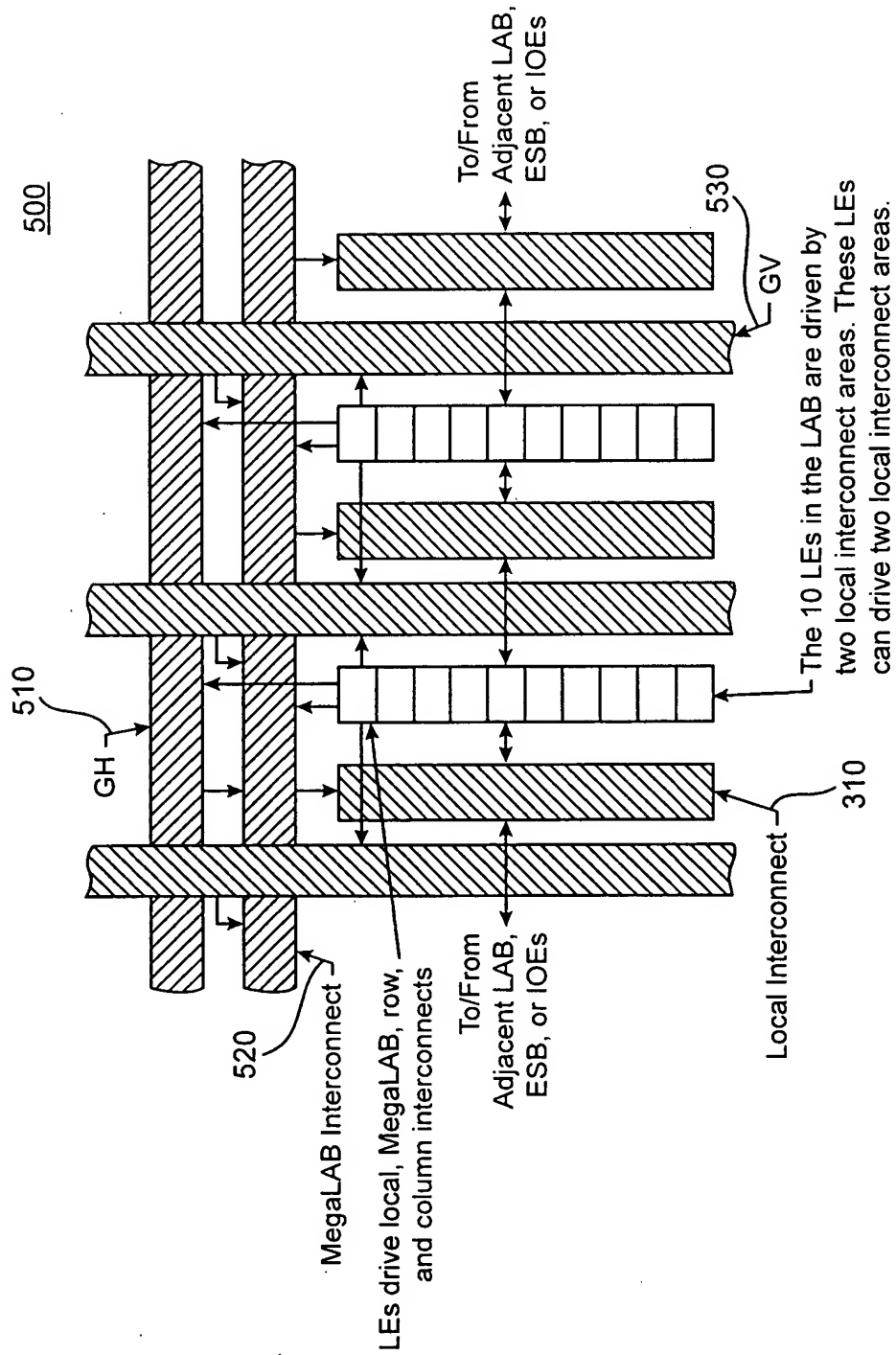


FIG. 5



5 / 30

600

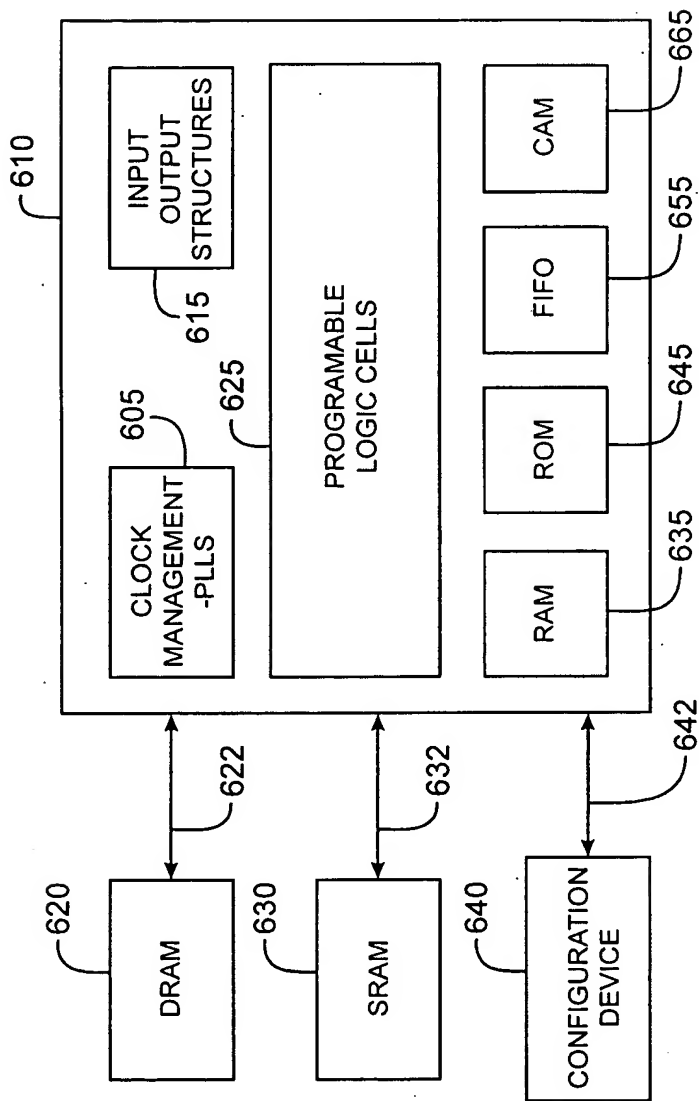
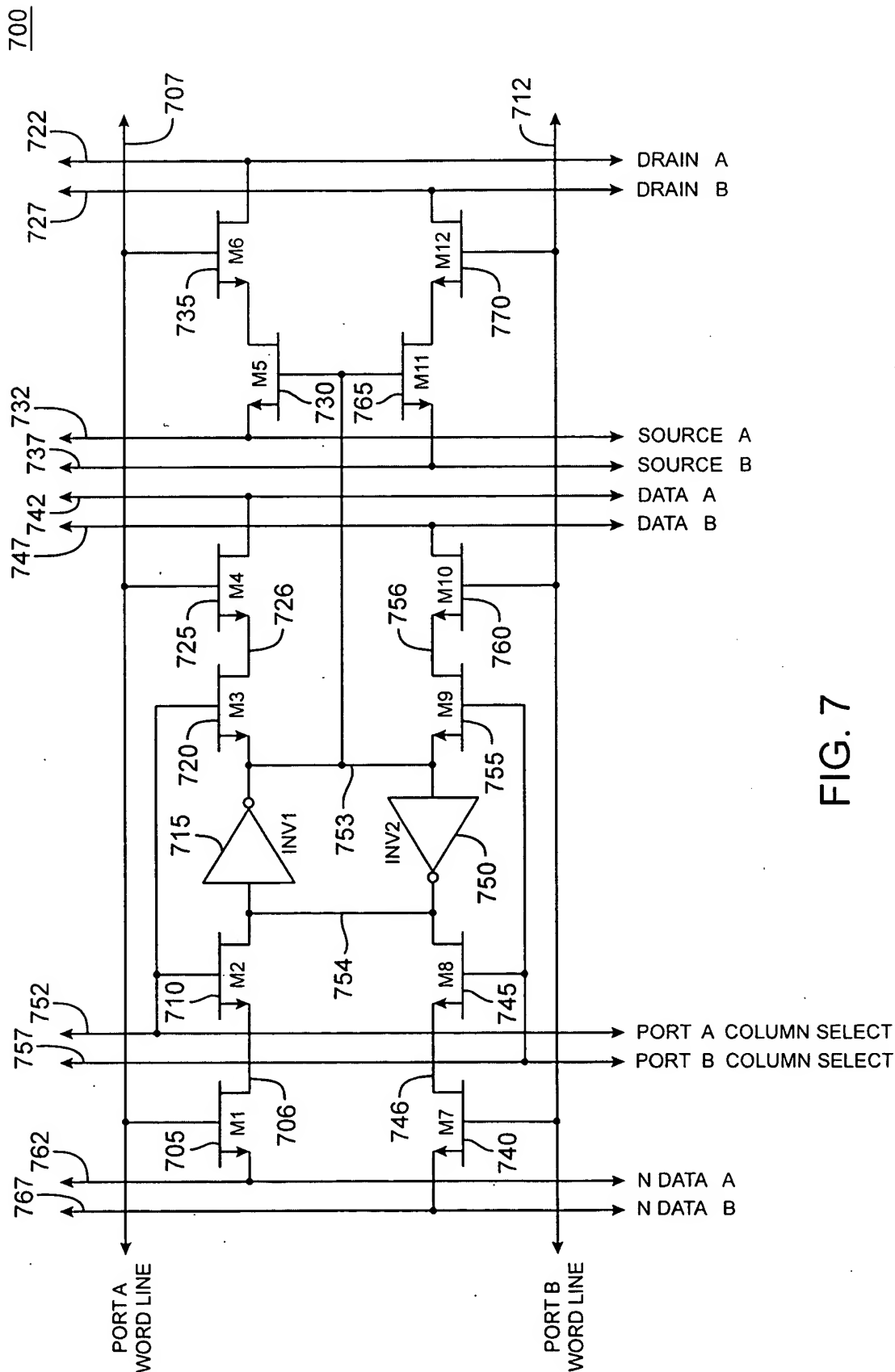


FIG. 6



6 / 30





7 / 30

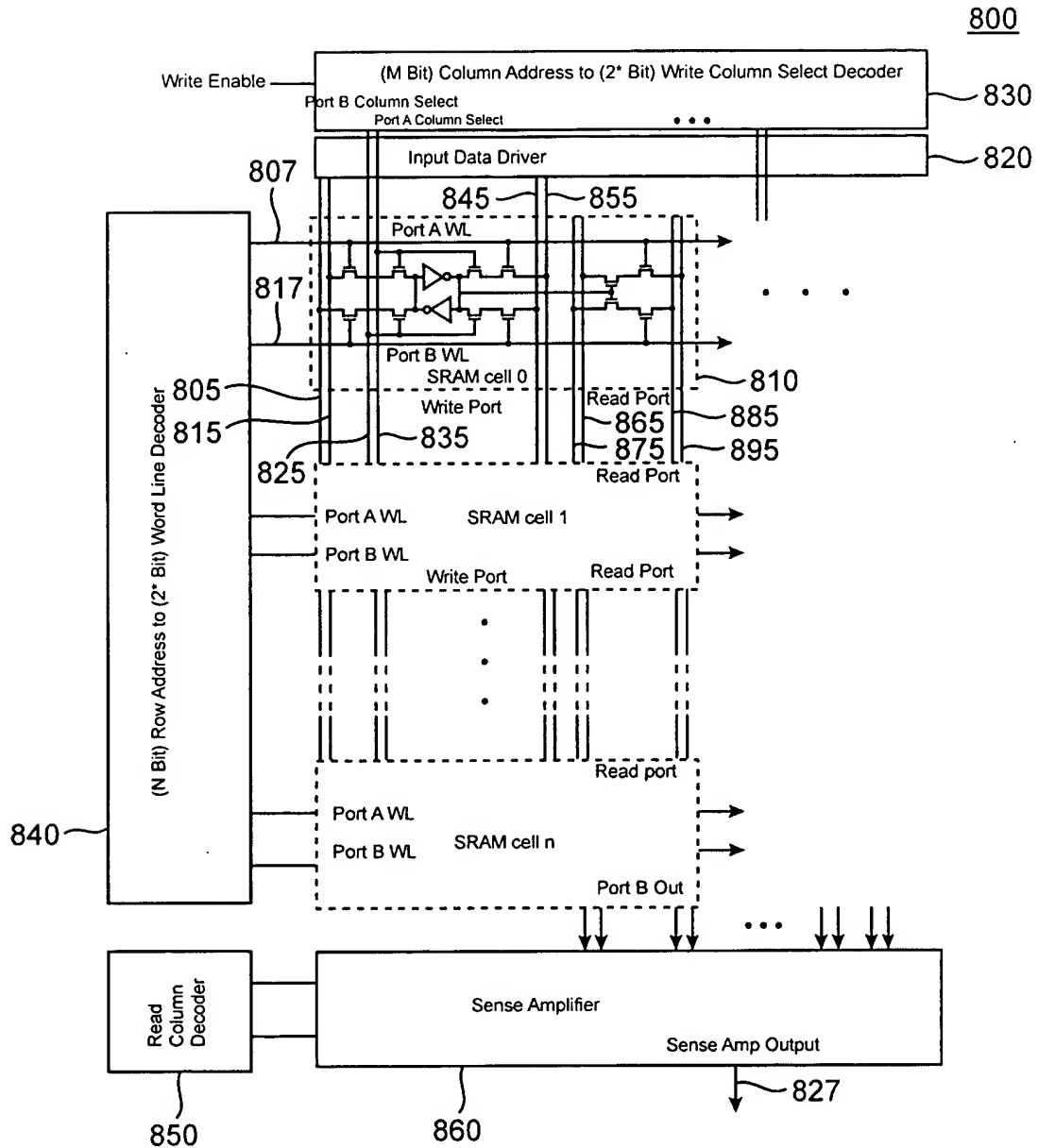


FIG. 8



900

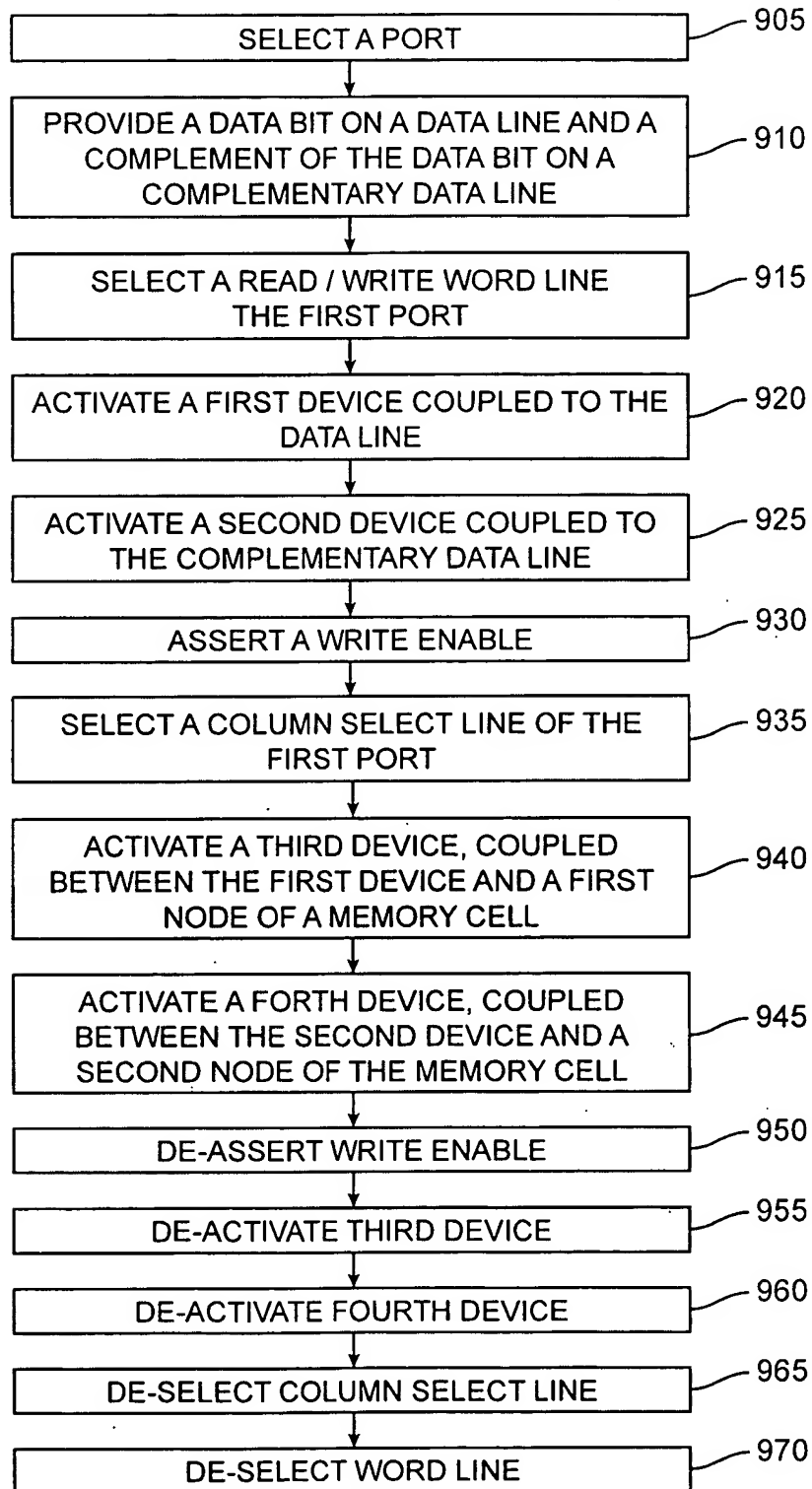


FIG. 9



1000

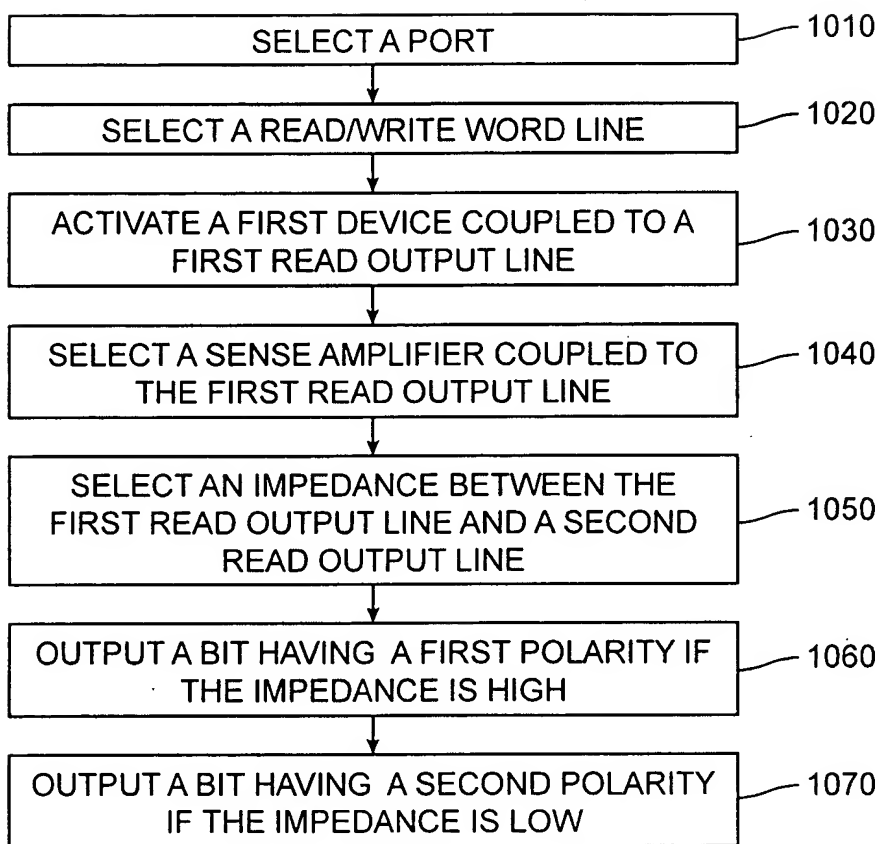


FIG. 10



10 / 30

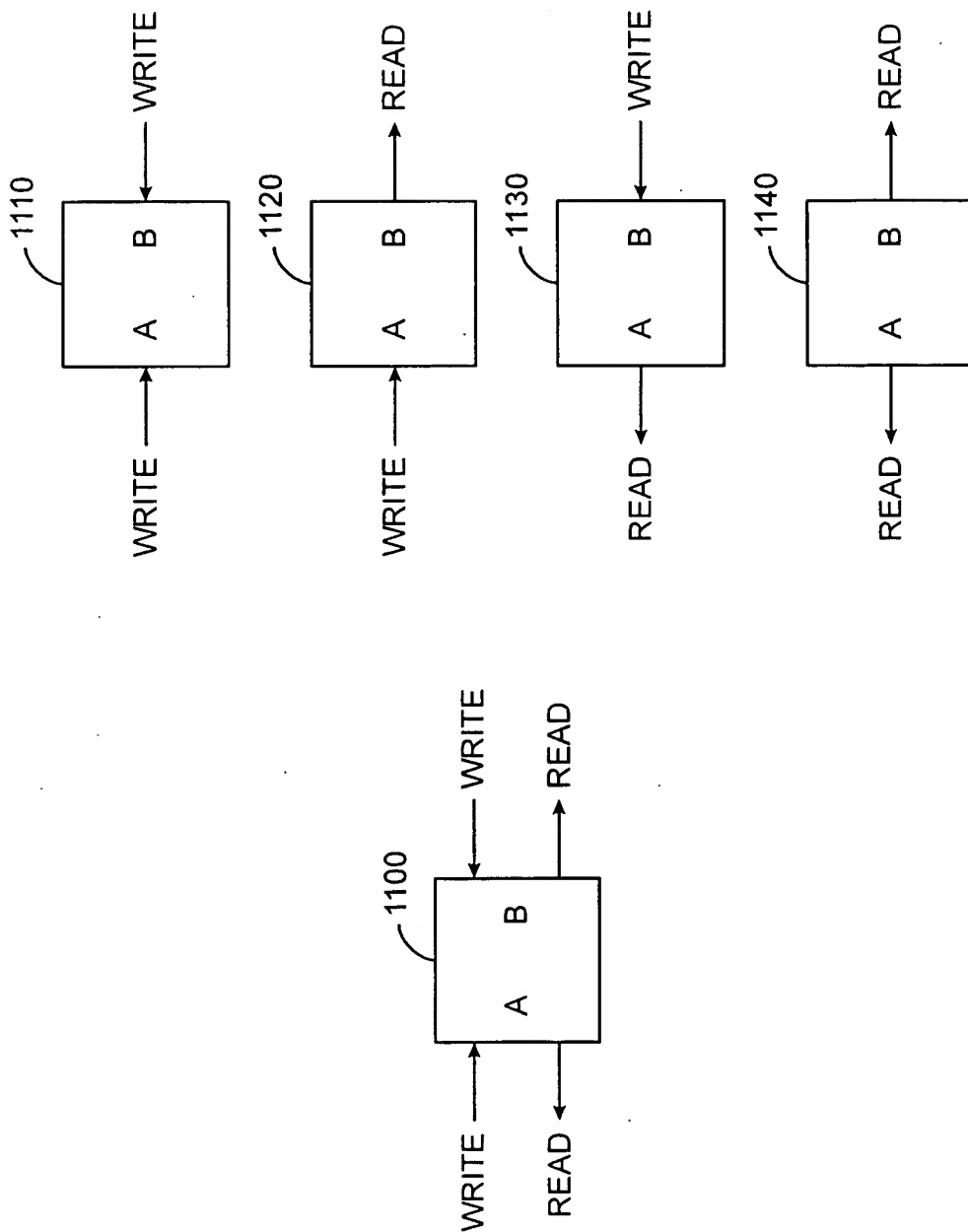


FIG. 11



1200

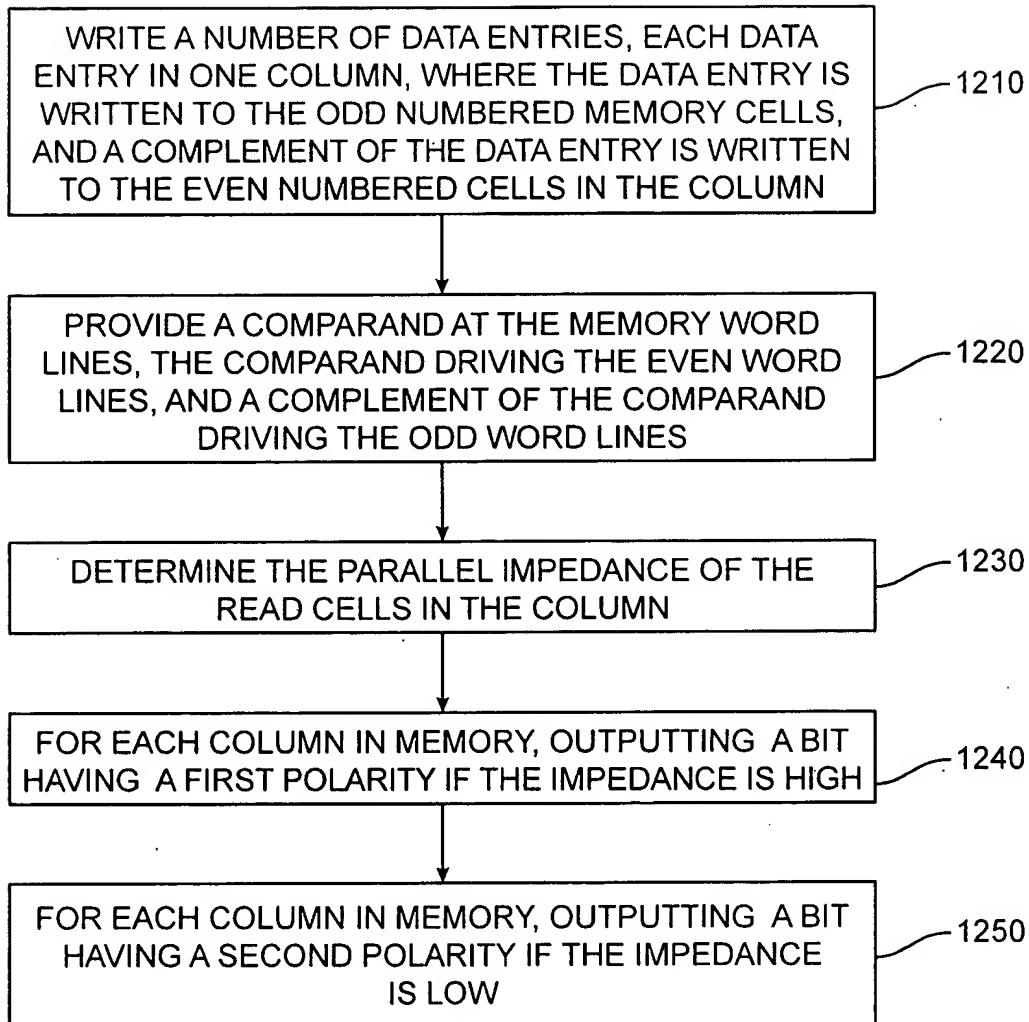


FIG. 12

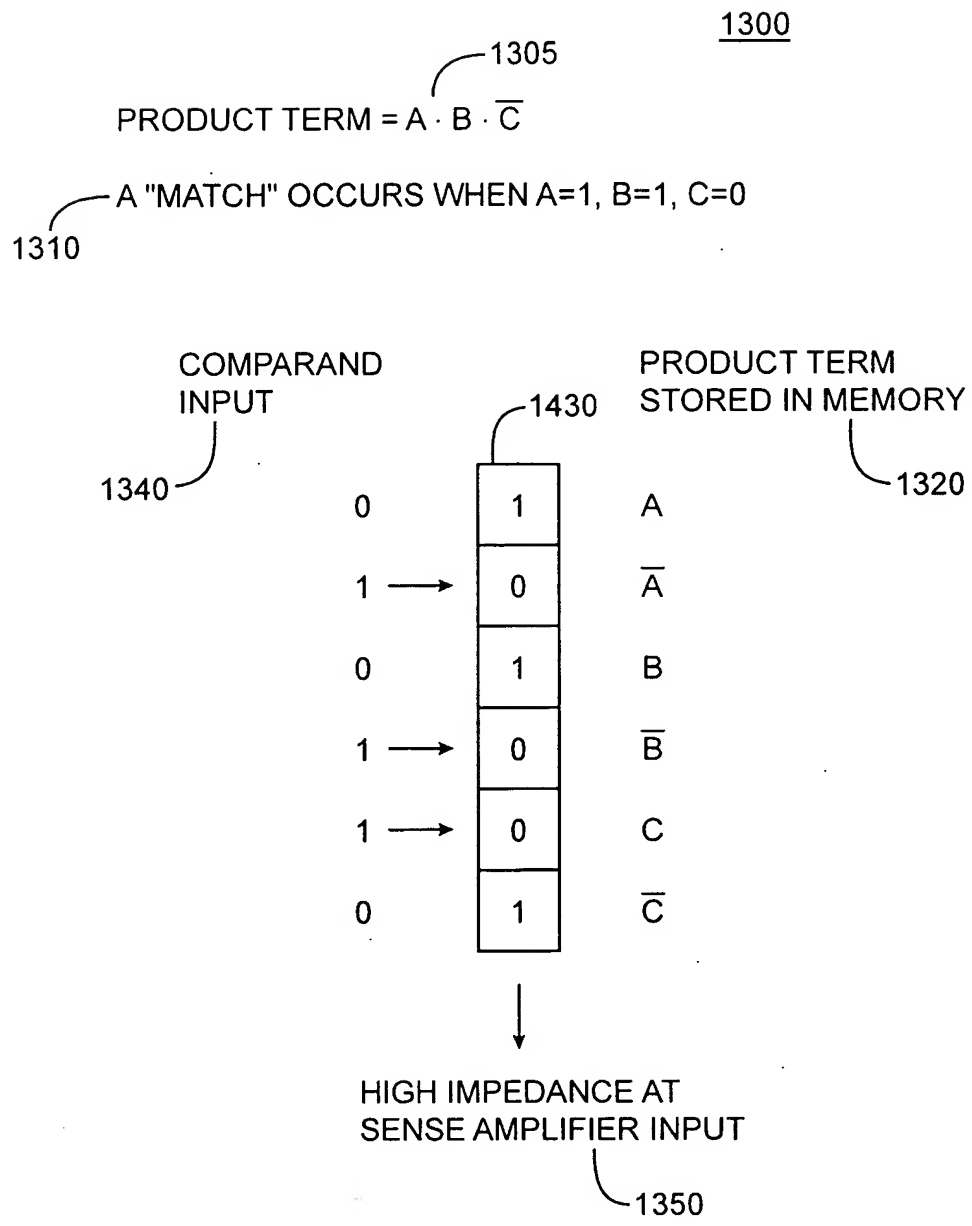


FIG. 13



13 / 30

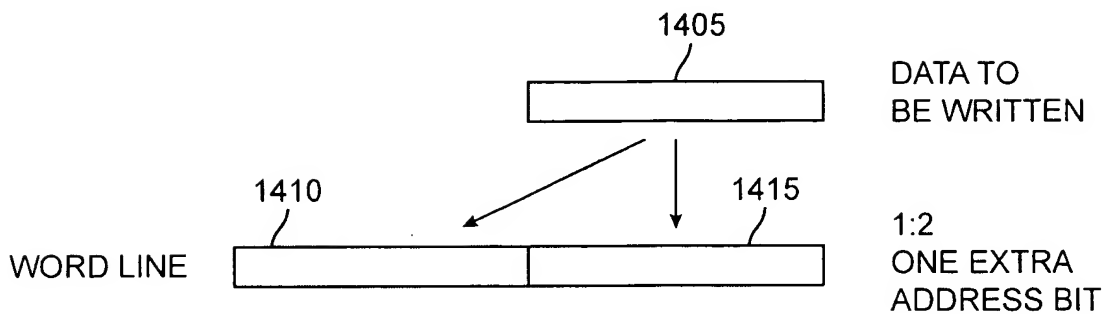


FIG. 14A

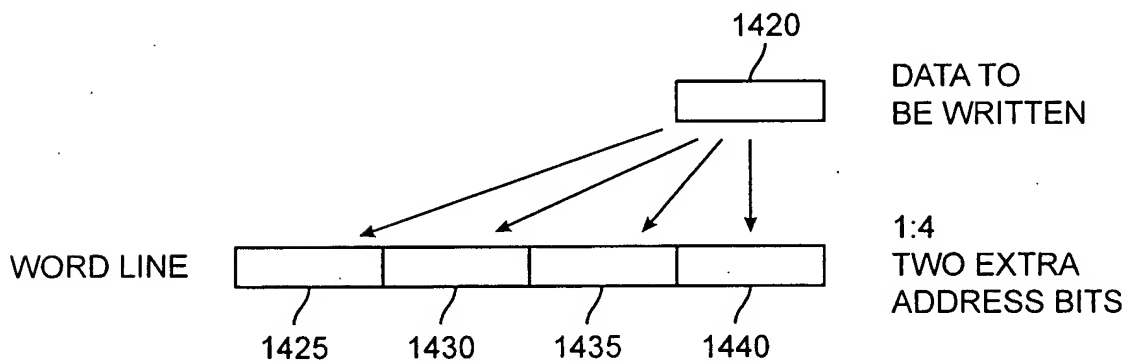


FIG. 14B

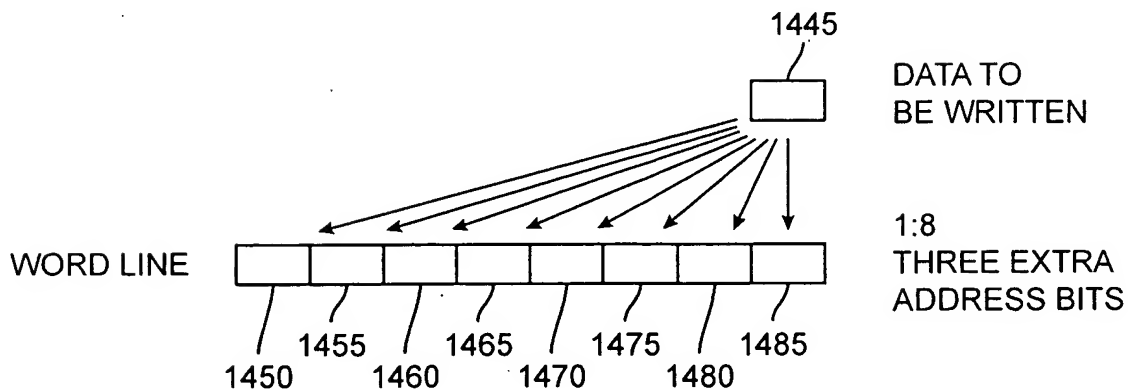


FIG. 14C



14 / 30

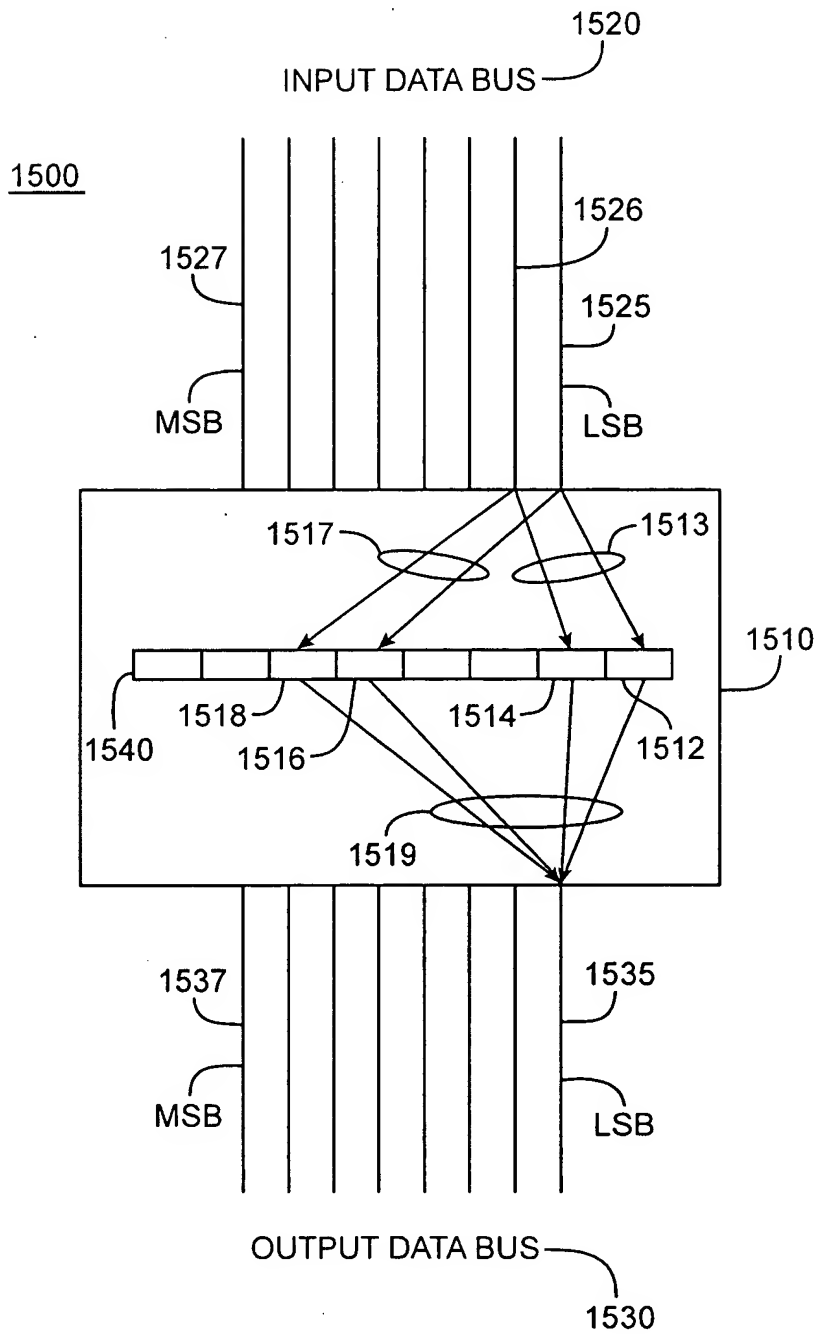


FIG. 15



15 / 30

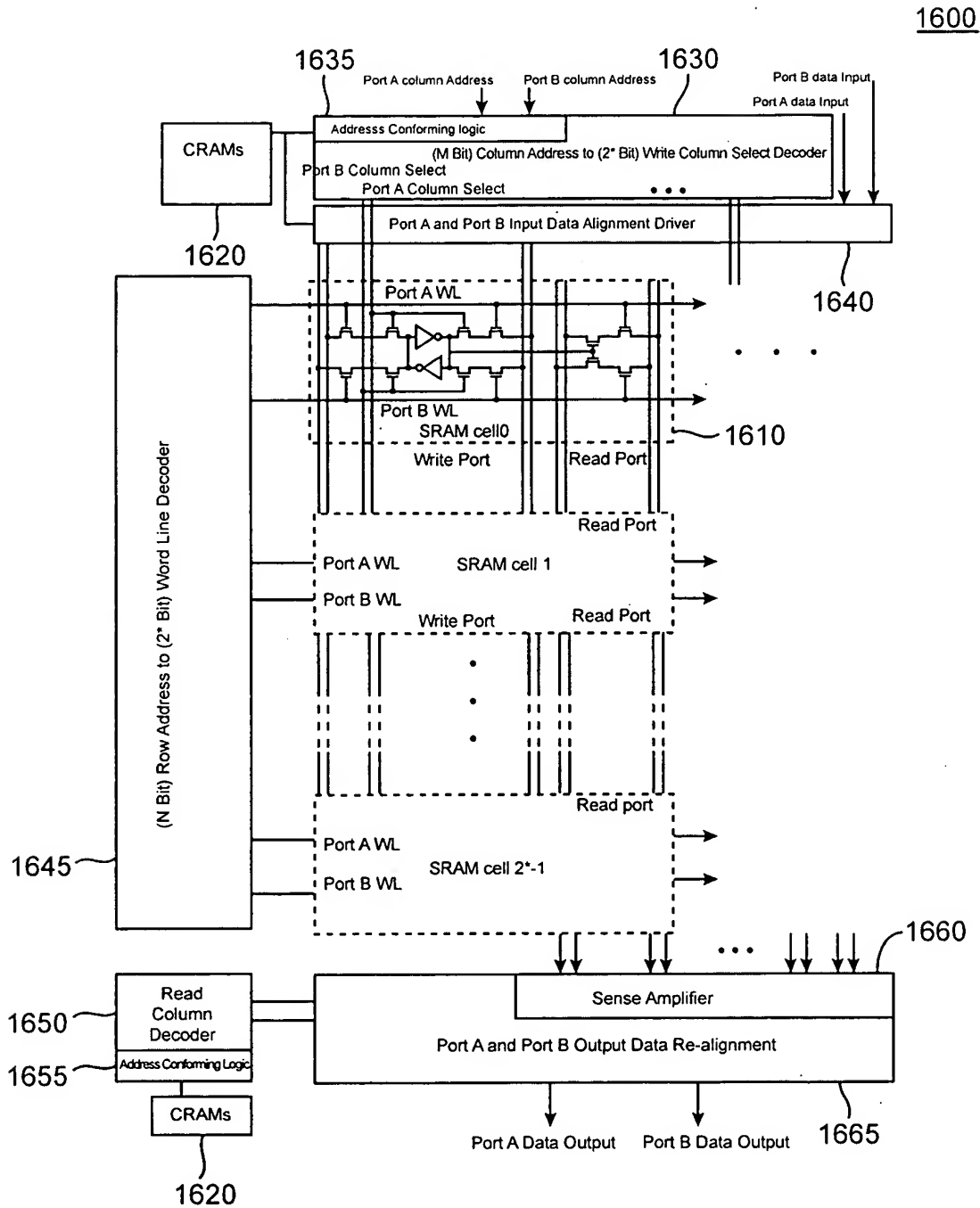


FIG. 16

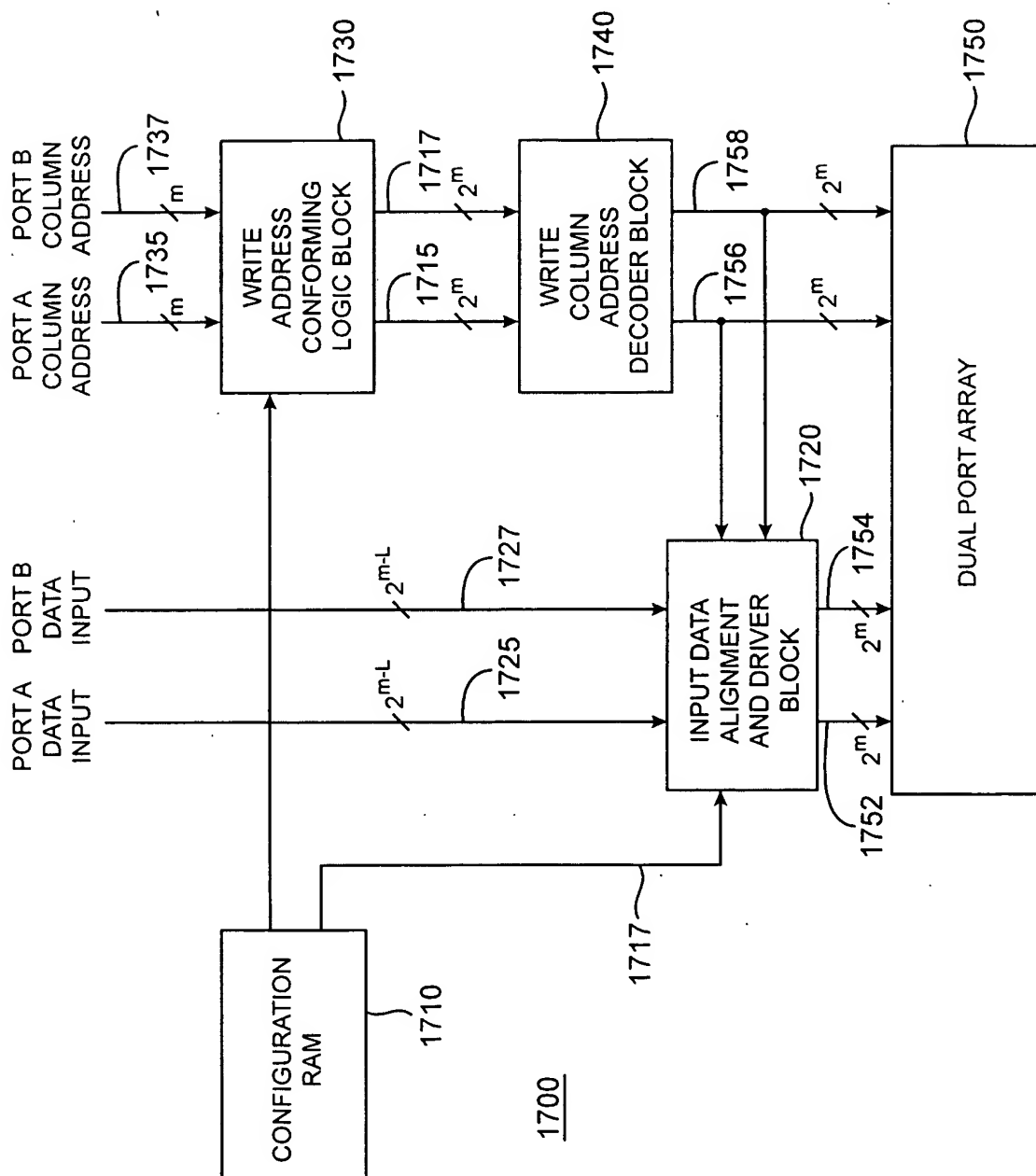


FIG. 17

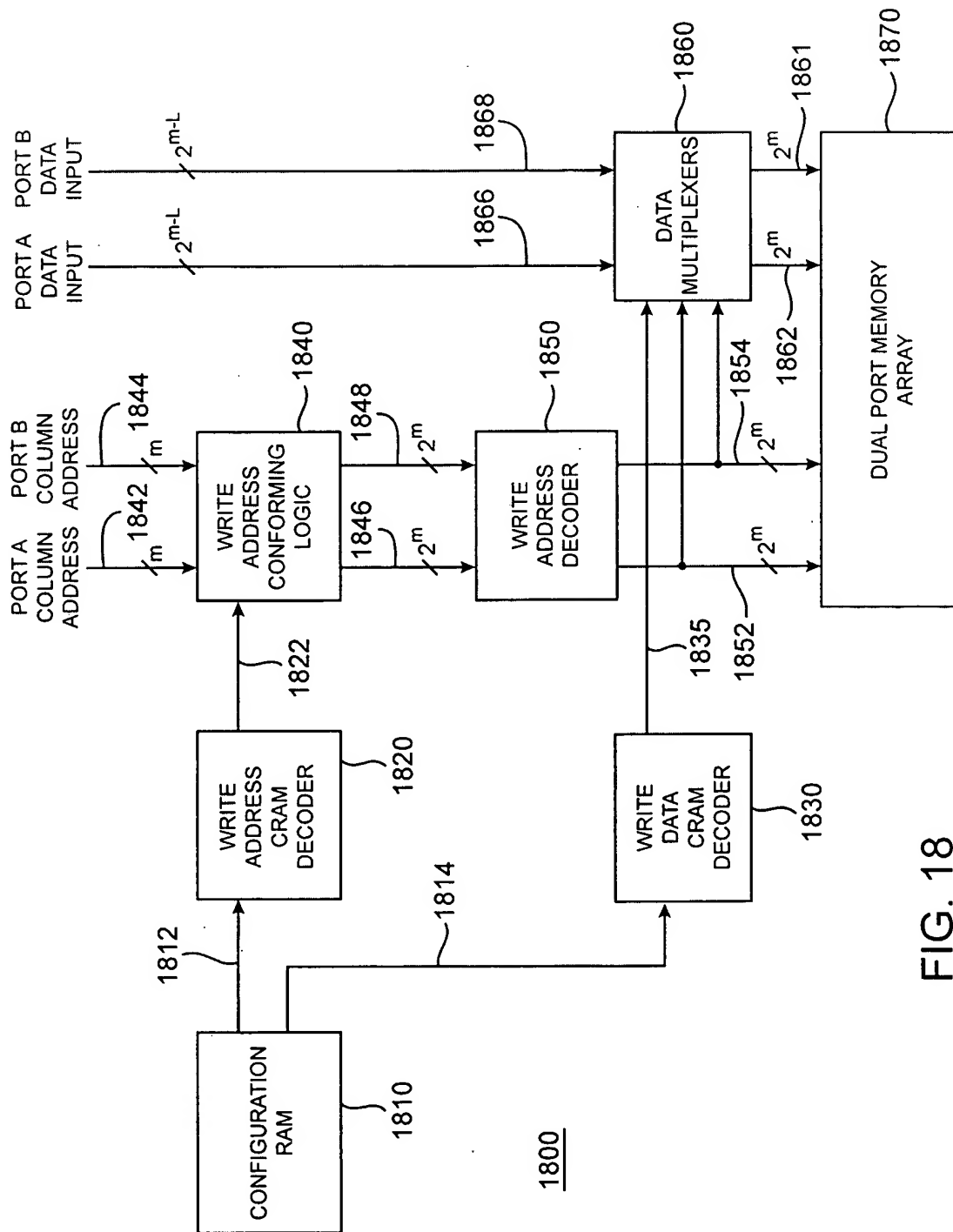


FIG. 18



18 / 30

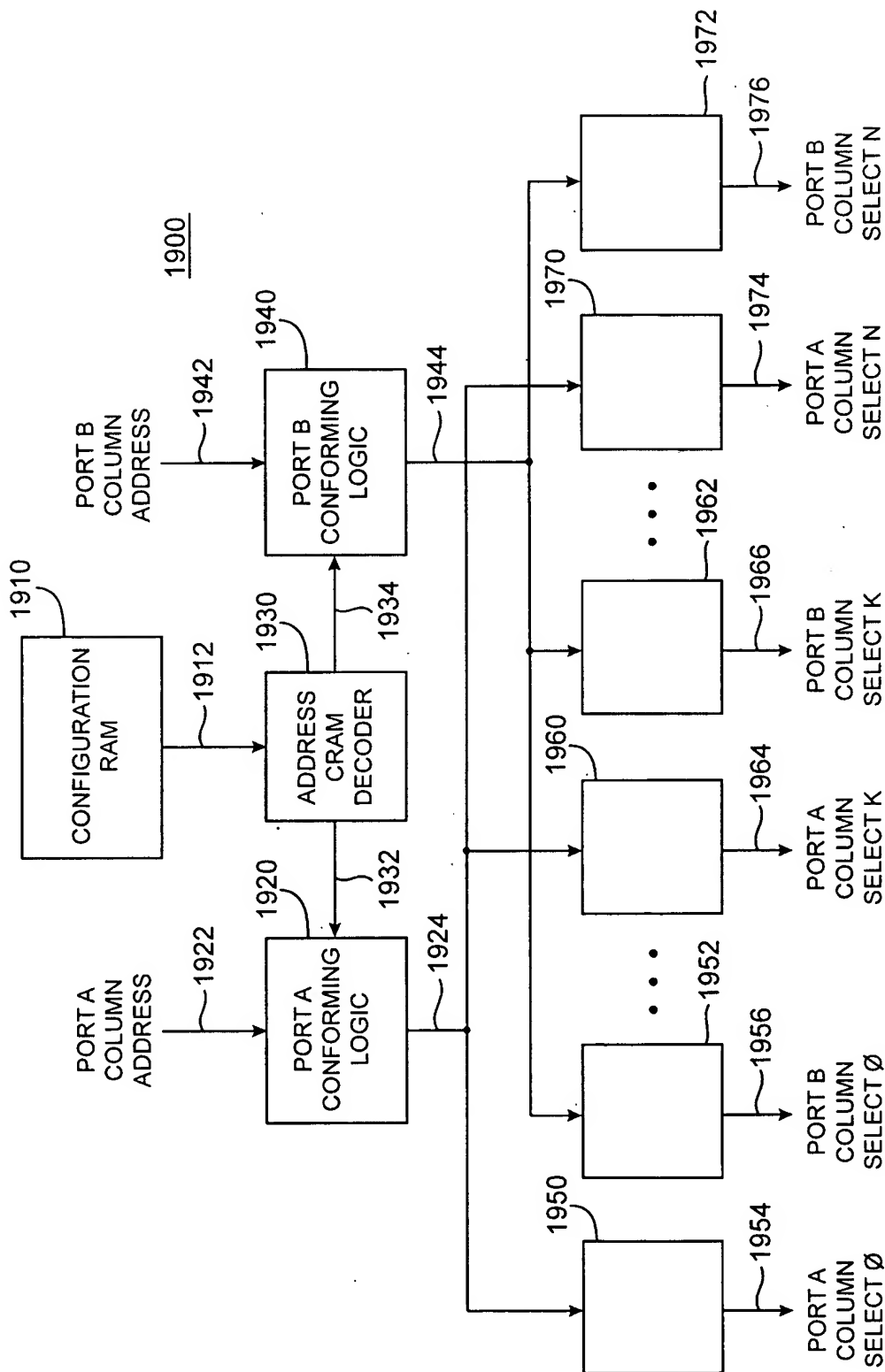
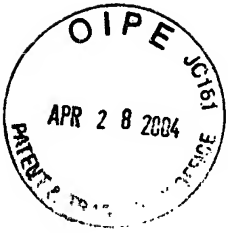


FIG. 19



19 / 30

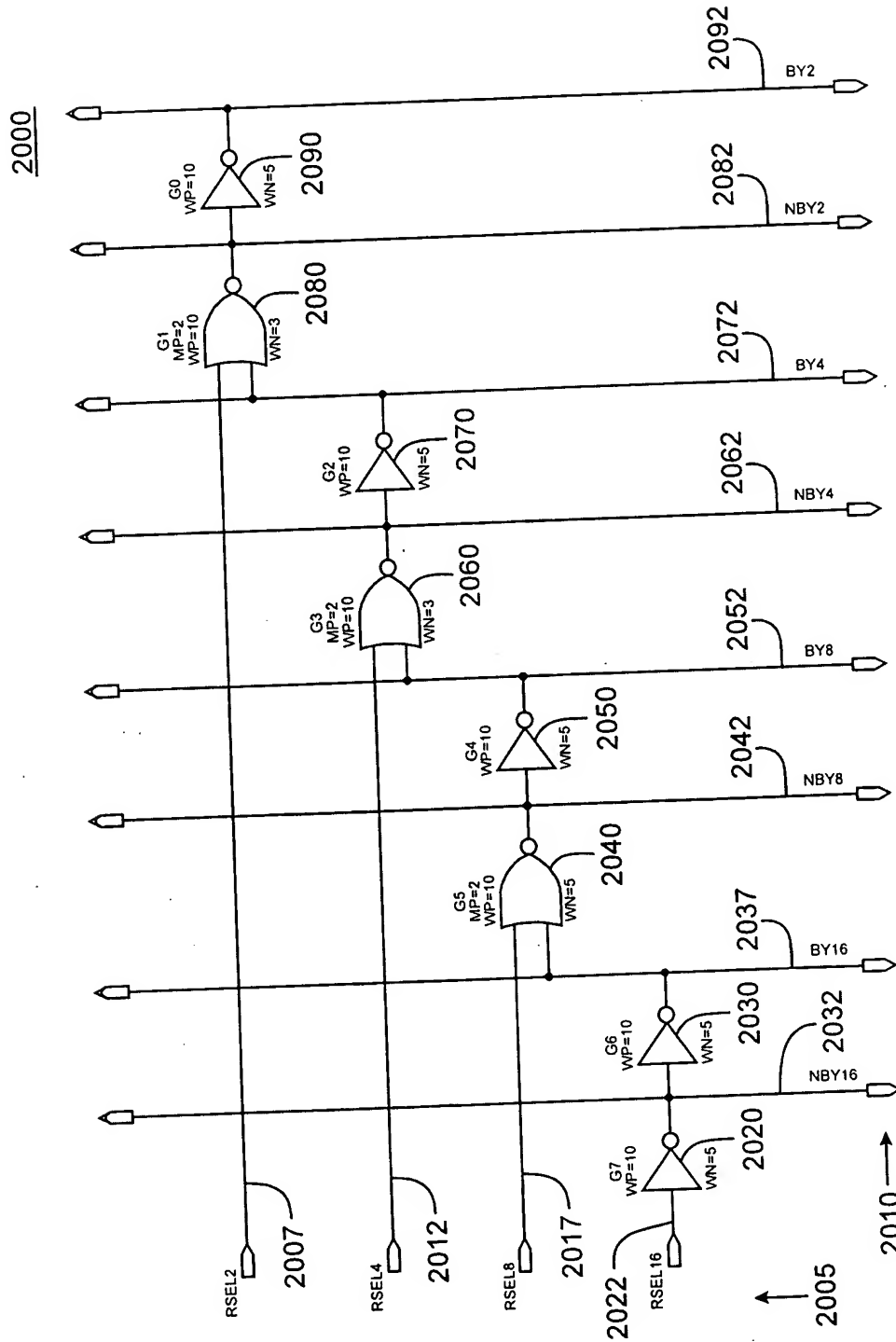


FIG. 20



20 / 30

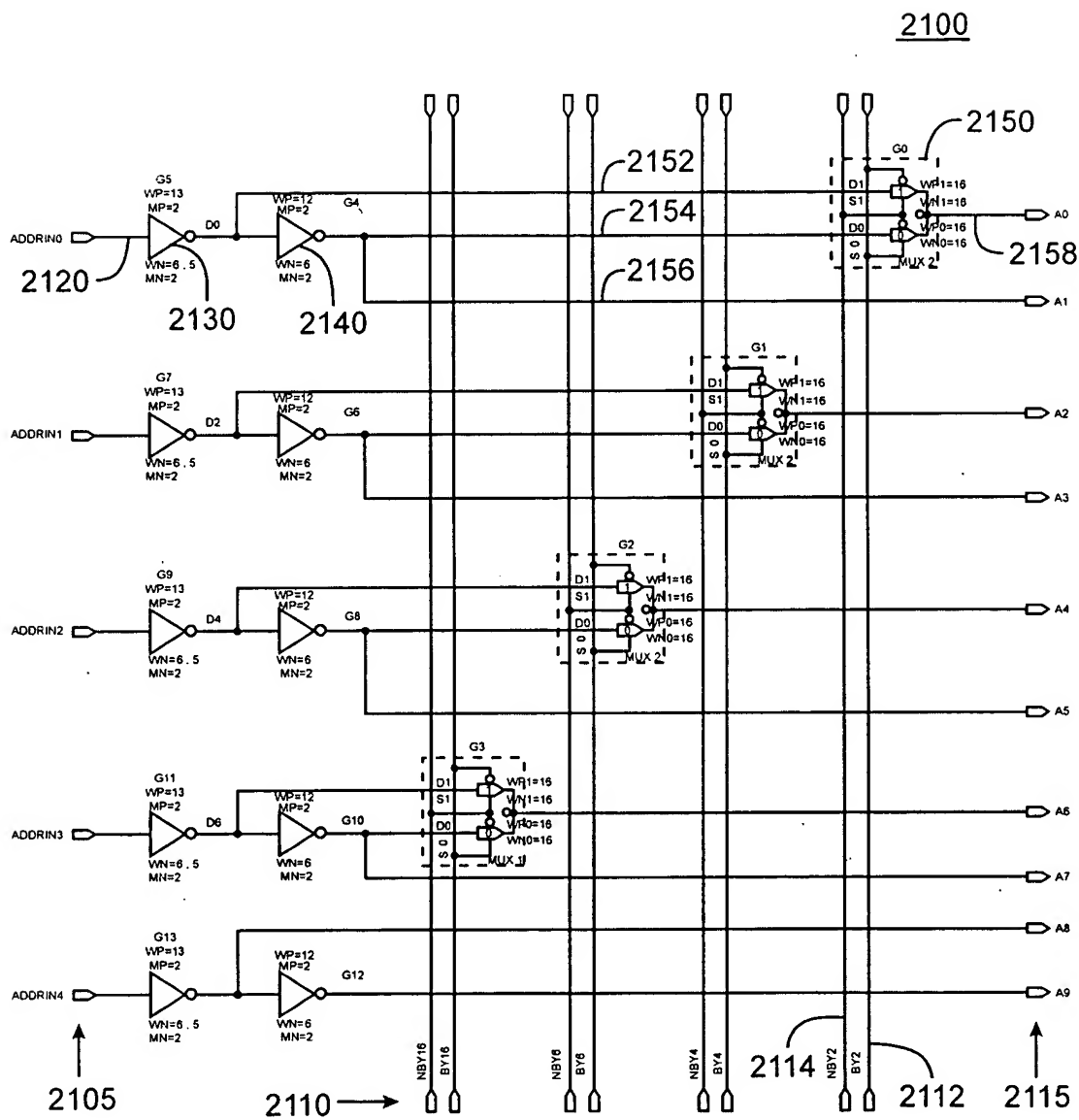


FIG. 21



21 / 30

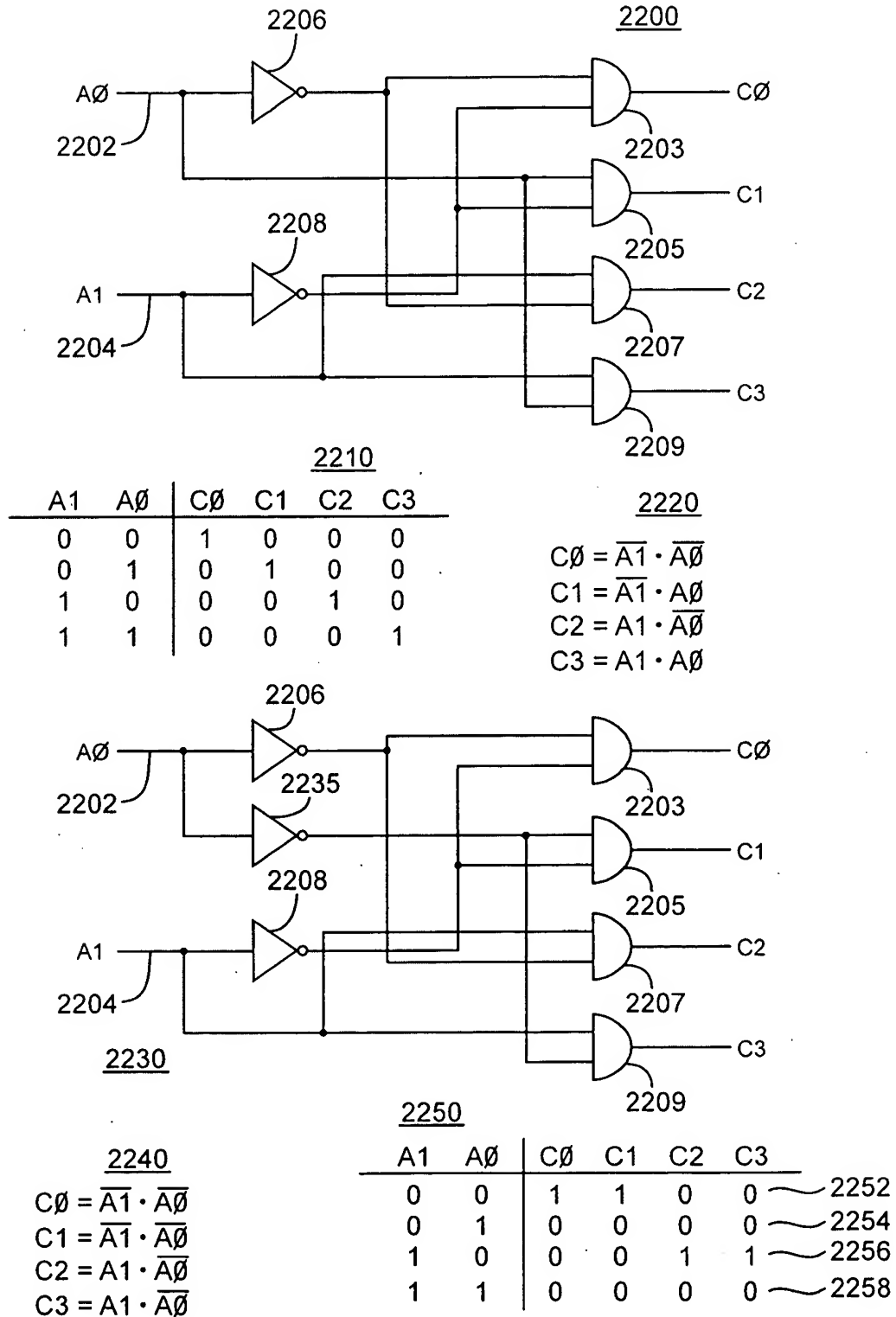
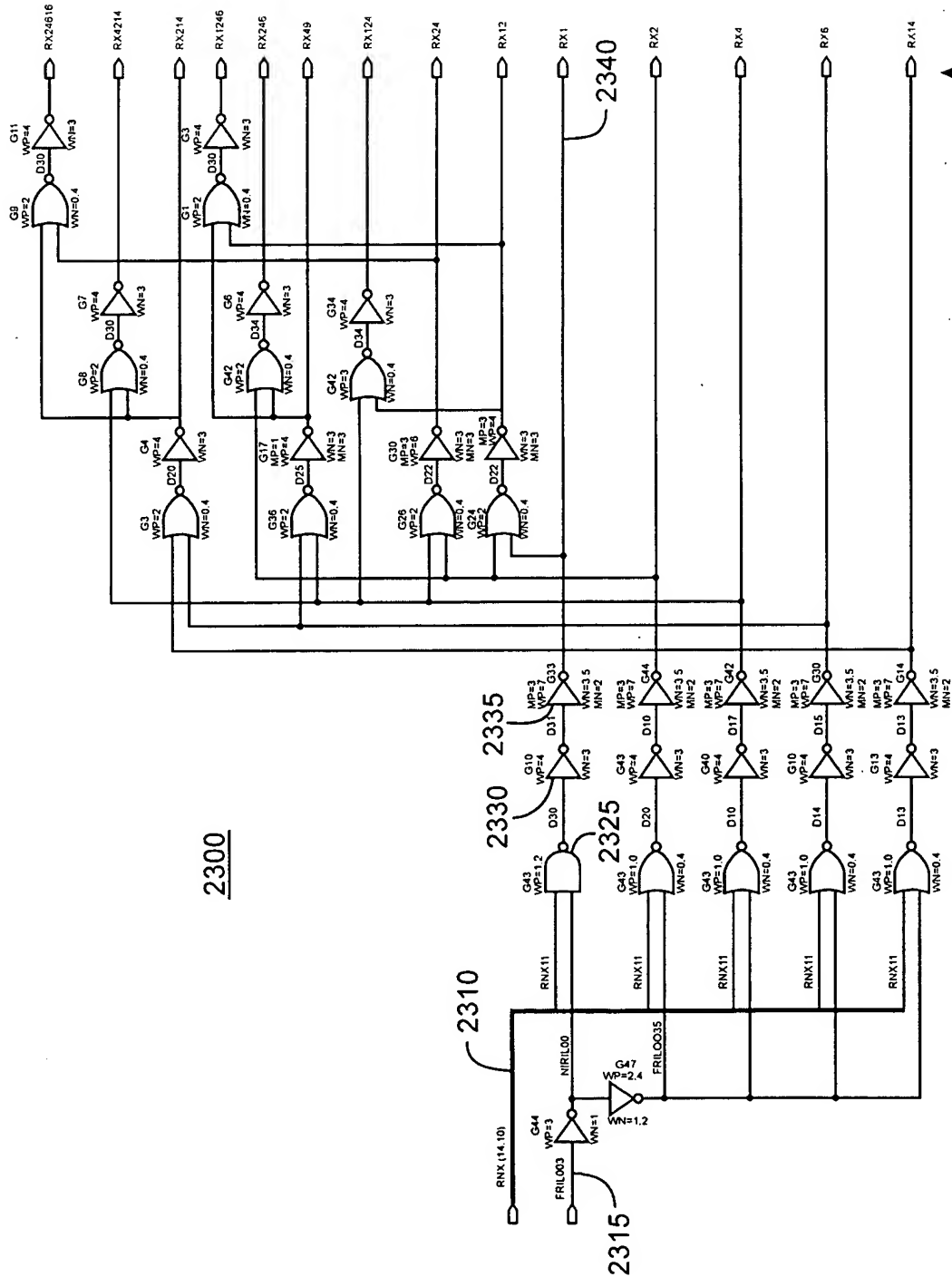
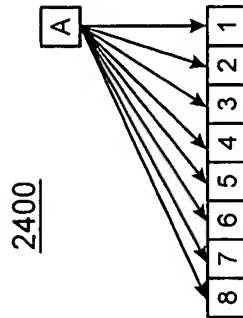
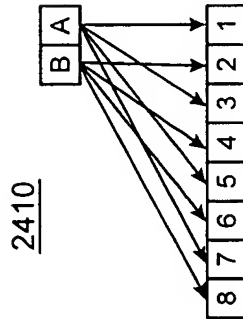
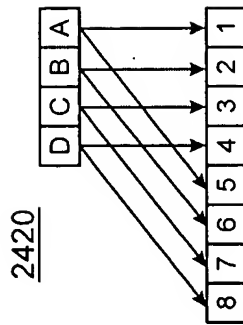


FIG. 22





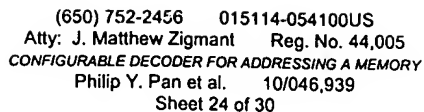
2430

MUX	# bits / word				INPUTS	TYPE MUX
	1	2	4			
1	A	A	A		A	1:1
2	A	B	B		A, B	2:1
3	A	A	C		A, C	2:1
4	A	B	D		A, B, D	3:1
5	A	A	A		A	1:1
6	A	B	B		A, B	2:1
7	A	A	C		A, C	2:1
8	A	B	D		A, B, D	3:1

2440

MUX	# bits / word				OUTPUTS	TYPE MUX
	1	2	4			
A	8, 7, 6, 5, 4, 3, 2, 1					1:8
B	8, 6, 4, 2					1:4
C	7, 3					1:2
D	8					1:1

FIG. 24





2600

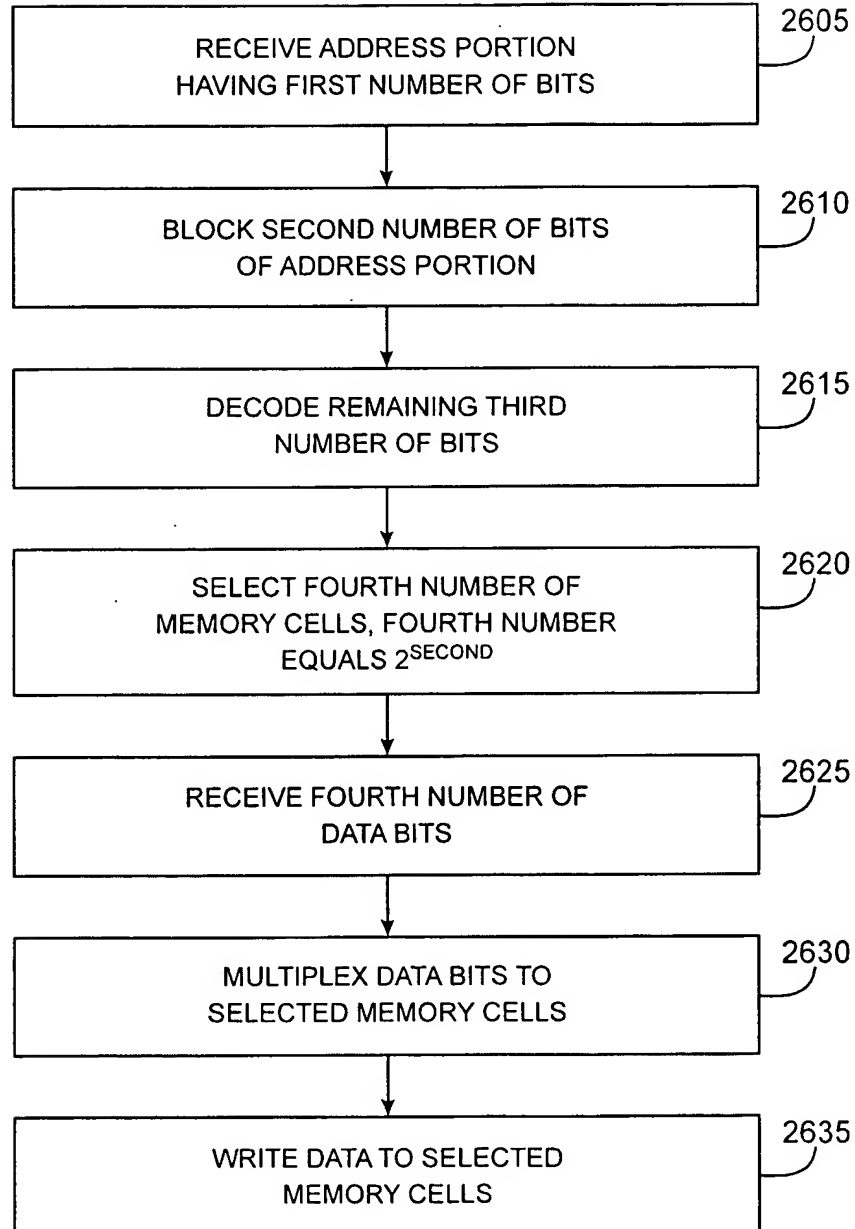
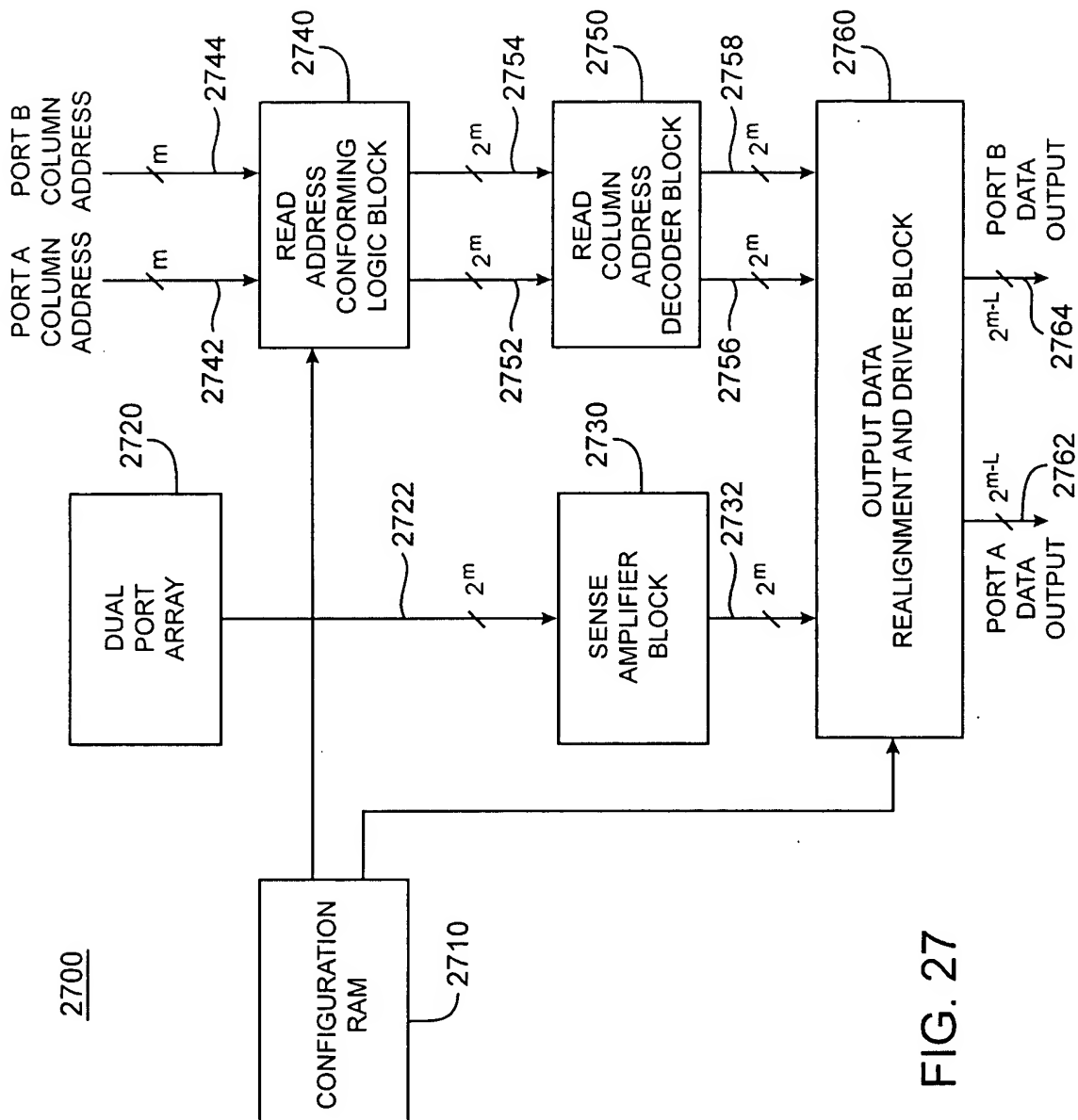


FIG. 26



26 / 30



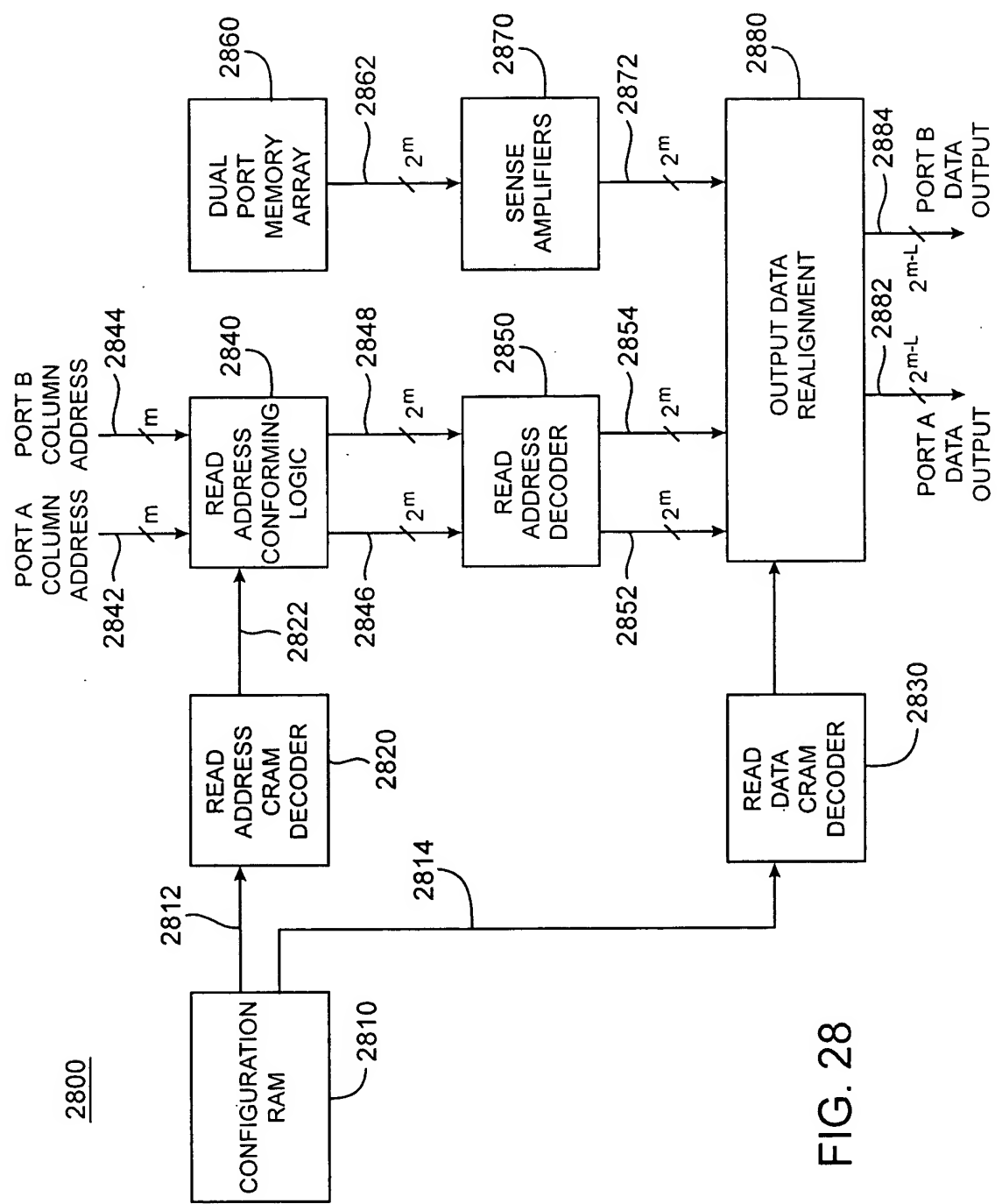
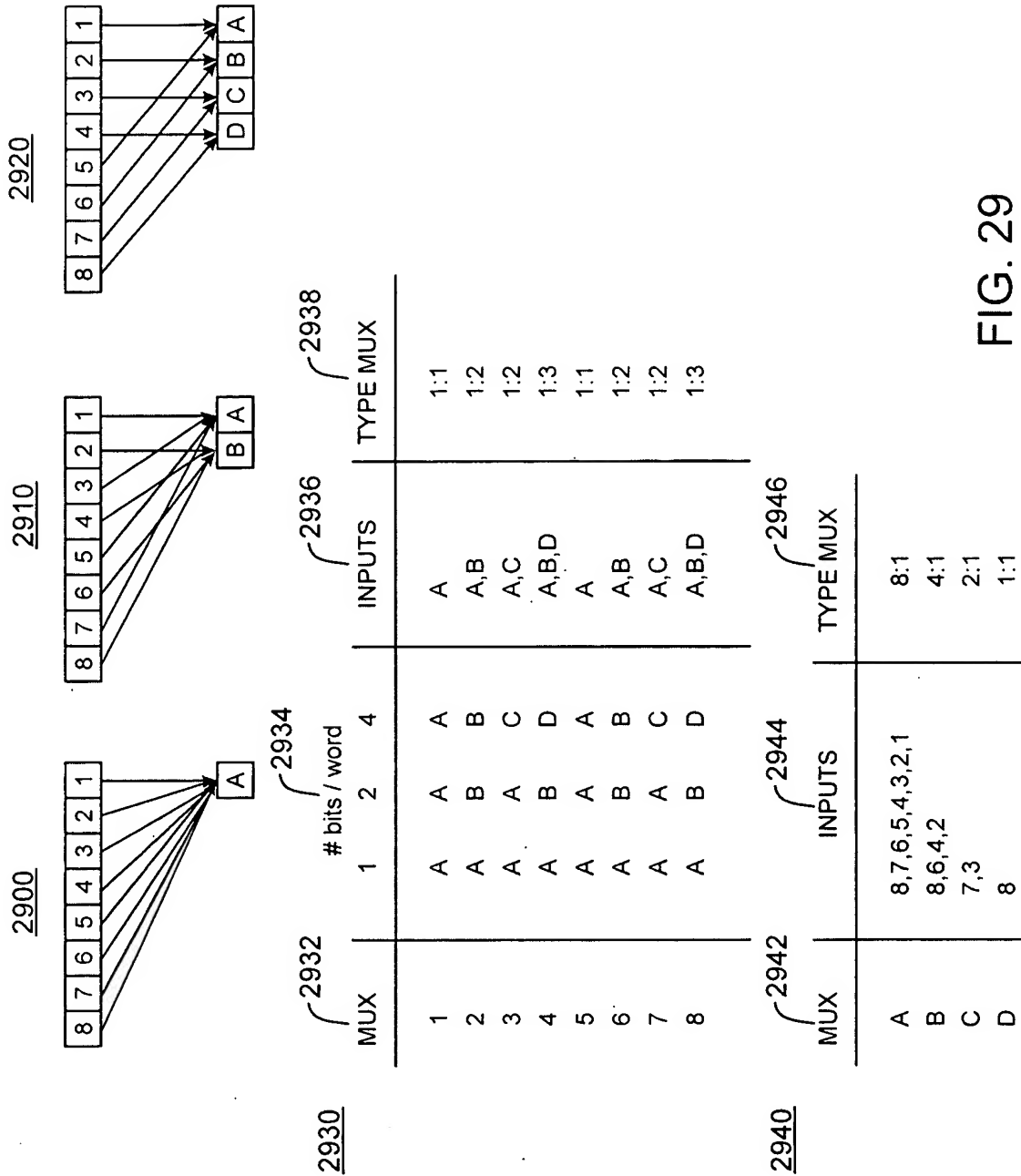
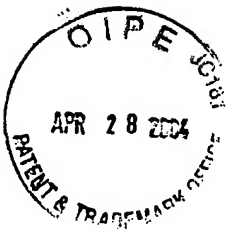


FIG. 28



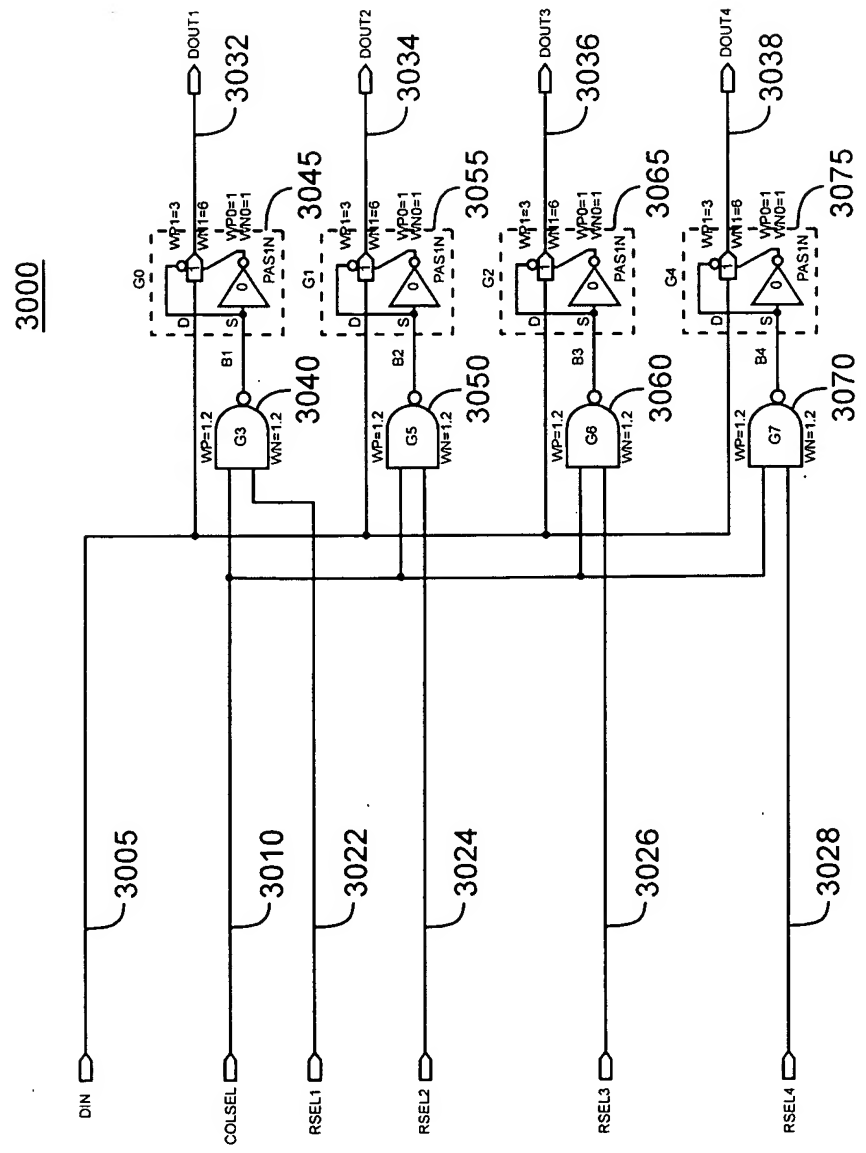


FIG. 30



30 / 30

3100

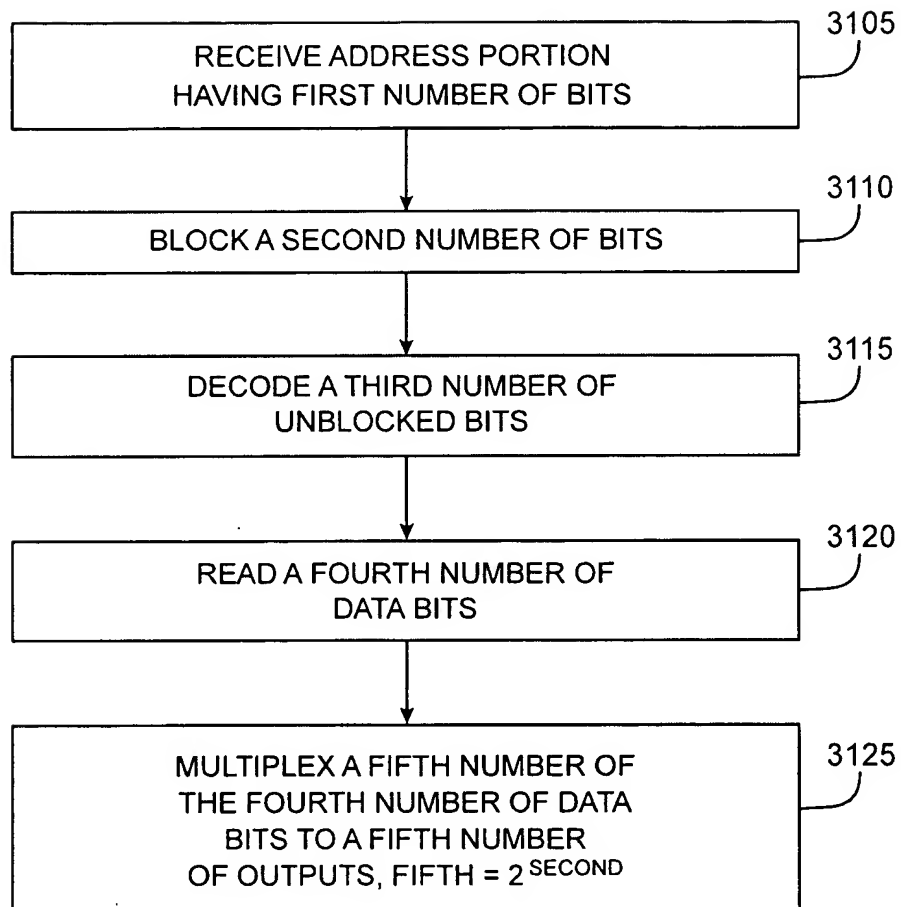


FIG. 31